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Claims

[c1] 1. A dynamic random access memory (DRAM) cell, comprising:
a semiconductor pillar disposed on a substrate;
a capacitor on a lower portion of a sidewall of the pillar, including a first plate in the lower portion of the sidewall of the pillar, a dielectric layer covering the lower portion of the sidewall of the pillar, and a second plate covering the dielectric layer; and
a vertical transistor on an upper portion of the sidewall of the pillar, including a first doped region in the sidewall coupled to the second plate of the capacitor, a second doped region in a top portion of the pillar, a gate on the sidewall between the first and the second doped regions, and a gate insulating layer between the sidewall and the gate.

[c2] 2. The DRAM cell of claim 1, wherein the first doped region and the gate surround the pillar.

[c3] 3. The DRAM cell of claim 1, wherein the second plate has a top portion directly contacting with the first doped region.

[c4] 4. The DRAM cell of claim 3, wherein the top portion of the second plate is separated from the gate by an insulator.

[c5] 5. The DRAM cell of claim 1, wherein the first plate, the dielectric layer and the second plate surround the pillar.

[c6] 6. The DRAM cell of claim 5, further comprising a collar insulating layer surrounding the pillar and covered by an upper portion of the second plate.

[c7] 7. The DRAM cell of claim 6, wherein the second plate includes a first conductor surrounding the collar insulating layer, a second conductor underlying the first conductor and the collar insulating layer, and a third conductor overlying the first conductor and the collar insulating layer and coupling with the first doped region.

[c8] 8. The DRAM cell of claim 1, wherein the gate is underlying an insulator that has a top surface approximately coplanar with the top surface of the pillar.

[c9] 9. A dynamic random access memory (DRAM) array, comprising:
rows and columns of memory cells disposed on a substrate, each comprising:
a semiconductor pillar on the substrate;
a capacitor on a lower portion of a sidewall of the pillar,

including a first plate in the lower portion of the sidewall of the pillar, a dielectric layer covering the lower portion of the sidewall of the pillar, and a second plate covering the dielectric layer; and

a vertical transistor on an upper portion of the sidewall of the pillar, including a first doped region in the sidewall coupled to the second plate of the capacitor, a second doped region in a top portion of the pillar, a gate on the sidewall between the first and the second doped regions, and a gate insulating layer between the sidewall and the gate;

a plurality of bit lines, each being coupled with the second doped regions of the memory cells in one row; and

a plurality of word lines, each being coupled with the gates of the memory cells in one column.

[c10] 10. The DRAM array of claim 9, wherein each bit line directly contacts with the second doped regions of the memory cells in one row.

[c11] 11. The DRAM array of claim 9, wherein the gates of the memory cells in one column are connected to each other to form a gate line.

[c12] 12. The DRAM array of claim 11, wherein the gate line directly serves as a word line.

[c13] 13. The DRAM array of claim 11, wherein a word line is electrically connected to the gate line via at least one contact between two pillars.

[c14] 14. The DRAM array of claim 13, wherein
the word lines cross over the bit lines; and
the DRAM array further comprises:
a cap layer on each bit line; and
a protective spacer on sidewalls of each pair of bit line and cap layer.

[c15] 15. The DRAM array of claim 9, wherein a first doped region and a gate of a memory cell surround a corresponding pillar.

[c16] 16. The DRAM array of claim 9, wherein the first plates of all memory cells are electrically connected via a doped surface layer of the substrate between the pillars to serve as a common electrode.

[c17] 17. The DRAM array of claim 9, wherein the second plate has a top portion directly contacting with a corresponding first doped region.

[c18] 18. The DRAM array of claim 17, wherein the top portion of the second plate is separated from a corresponding gate by an insulator.

[c19] 19. The DRAM array of claim 9, wherein the first plate, the dielectric layer and the second plate surround the pillar.

[c20] 20. The DRAM array of claim 19, further comprising a collar insulating layer surrounding the pillar and covered by an upper portion of the second plate.

[c21] 21. The DRAM array of claim 20, wherein the second plate includes a first conductor surrounding the collar insulating layer, a second conductor underlying the first conductor and the collar insulating layer, and a third conductor overlying the first conductor and the collar insulating layer and coupling with a corresponding first doped region.

[c22] 22. The DRAM array of claim 9, wherein each gate underlies an insulator that has a top surface approximately coplanar with the top surface of a corresponding pillar.

[c23] 23. A method for fabricating a DRAM array, comprising:
patterning a semiconductor substrate to form rows and columns of pillars thereon;
forming a capacitor on a lower portion of a sidewall of each pillar;
partially filling spaces between the pillars with a first insulating material to cover the capacitors;

forming a gate structure of a transistor on the sidewall of each pillar above the first insulating layer, the gate structure comprising a gate electrode and a gate insulating layer between the pillar and the gate electrode;
forming a first doped region of a transistor in the sidewall of each pillar coupling with the capacitor on the sidewall of the same pillar;
forming a second doped region of a transistor in a top portion of each pillar;
filling the spaces between the pillars with a second insulating material to cover the transistors;
forming a plurality of bit lines over the substrate, wherein each bit line is electrically connected to the second doped regions of the transistors in one row; and
forming a plurality of word lines over the substrate, wherein each word line is coupled with the gates of the transistors in one column.

[c24] 24. The method of claim 23, wherein forming the capacitor on the lower portion of the sidewall of each pillar comprises:
doping a surface layer of the substrate and the lower portions of the sidewalls of the pillars to form a common electrode;
forming a dielectric layer surrounding the lower portion of the sidewall of each pillar; and

forming an upper electrode covering the dielectric layer for coupling with a corresponding first doped region.

[c25] 25. The method of claim 24, wherein a top of the upper electrode is higher than a top of the dielectric layer, and forming the capacitor on the lower portion of the sidewall of each pillar further comprises:
forming a collar insulating layer on the sidewall of the pillar above the dielectric layer before the upper electrode is formed, so that the collar insulating layer surrounds the pillar and is covered by an upper portion of the upper electrode.

[c26] 26. The method of claim 25, wherein the upper electrode comprises a doped semiconductor material, and a top portion of the upper electrode above the collar insulating layer directly contacts with the pillar, so that the first doped region is formed via dopant diffusion from the top portion of the upper electrode to the sidewall of the pillar during thermal processes after the upper electrode is formed.

[c27] 27. The method of claim 26, wherein forming the dielectric layer, the upper electrode and the collar insulating layer comprises:
forming a conformal dielectric layer on the substrate and the pillars;

forming a first conductive layer between the pillars to cover a lower portion of the conformal dielectric layer;
removing the dielectric layer exposed by the first conductive layer;
forming an insulating spacer on the sidewall of each pillar above the first conductive layer;
forming a second conductive layer between the pillars to cover lower portions of the insulating spacers;
removing a portion of each insulating spacer exposed by the second conductive layer to form a collar insulating layer on each pillar;
forming a third conductive layer between the pillars and on the collar insulating layers and the second conductive layer;
forming a mask spacer on the sidewall of each pillar above the third conductive layer; and
sequentially etching the third conductive layer, the second conductive layer and the first conductive layer using the mask spacer as a mask to form an upper electrode for each pillar.

[c28] 28. The method of claim 26, wherein forming the dielectric layer, the upper electrode and the collar insulating layer comprises:
forming a conformal dielectric layer on the substrate and the pillars;

forming a conductive spacer on the sidewall of each pillar covering a portion of the conformal dielectric layer;
forming an insulating layer between the pillars to cover lower portions of the conductive spacers;
removing portions of the conductive spacers and the dielectric layer exposed by the insulating layer;
forming an insulating spacer on the sidewall of each pillar above the insulating layer, the insulating spacer exposing a portion of a top surface of a corresponding conductive spacer;
forming a second conductive layer between the pillars to cover lower portions of the insulating spacers;
removing a portion of each insulating spacer exposed by the second conductive layer to form a collar insulating layer on the sidewall of each pillar;
forming a third conductive layer between the pillars and on the collar insulating layers and the second conductive layer;
forming a mask spacer on the sidewall of each pillar above the third conductive layer; and
sequentially etching the third conductive layer and the second conductive layer using the mask spacer as a mask to form an upper electrode for each pillar, wherein the upper electrode includes a conductive spacer, a portion of the second conductive layer and a portion of the third conductive layer.

[c29] 29. The method of claim 23, wherein forming the gate structure of the transistor on the sidewall of each pillar above the first insulating layer comprises:
forming a gate insulating layer on the sidewall of each pillar above the first insulating material;
forming a conductive layer between the pillars and on the first insulating material, the conductive layer having a top surface lower than the top surface of the pillar;
forming a mask spacer on the sidewall of each pillar above the conductive layer;
forming a mask layer comprising a plurality of linear patterns over the substrate, wherein each linear pattern runs over the pillars in one column; and
etching the conductive layer using the mask spacer and the mask layer as a mask to form a gate electrode on the sidewall of each pillar, wherein the gate electrodes on the pillars in one column are connected via the conductive layer between the pillars of the same column to form a gate line.

[c30] 30. The method of claim 29, wherein a gate line directly serves as a word line for the transistors in one column.

[c31] 31. The method of claim 29, wherein a word line is formed crossing over the bit lines to electrically connect a corresponding gate line via at least one contact be-

tween the pillars of the corresponding column.

[c32] 32. The method of claim 23, wherein forming the gate structure of the transistor on the sidewall of each pillar above the first insulating layer comprises:
forming a gate insulating layer on the sidewall of each pillar above the first insulating material;
forming a conformal conductive layer on the pillars and the first insulating material, also covering the gate insulating layer;
forming a first mask layer between the pillars to cover a lower portion of the conformal conductive layer;
forming a second mask layer comprising a plurality of linear patterns on the conformal conductive layer and the first mask layer, wherein each linear pattern runs over the pillars in one column;
removing portions of the first mask layer exposed by the second mask layer;
removing the second mask layer; and
anisotropically etching the conformal conductive layer using the remaining first mask layer as a mask until a top of the conductive layer is substantially lower than the top surface of the pillar, so as to form a spacer-like gate electrode on the sidewall of each pillar, wherein the gate electrodes on the pillars in one column are connected via the conductive layer between the pillars of the same col-

umn to form a gate line.

[c33] 33. The method of claim 32, wherein the gate line directly serves as a word line for the transistors in one column.

[c34] 34. The method of claim 32, wherein a word line is formed crossing over the bit lines to electrically connect the corresponding gate line via at least one contact between the pillars of the corresponding column.

[c35] 35. The method of claim 23, wherein each bit line directly contacts with the second doped regions of the transistors in one row.

[c36] 36. The method of claim 23, wherein the gate electrodes on the pillars of one column are connected via the conductive layer between the pillars of the same column to form the gate line, and the step of forming the word lines comprises:
forming a dielectric layer over the substrate covering the bit lines; and
forming at least one contact through the dielectric layer and a word line on the dielectric layer to electrically connect with the gate line, wherein the contact directly contacts the conductive layer between two pillars of the same column.

[c37] 37. The method of claim 36, wherein
each bit line is formed with a cap layer thereon; and
the method further comprises:
forming a protective spacer on sidewalls of each pair of bit line and cap layer before the dielectric layer is formed.

[c38] 38. The method of claim 36, wherein the contact and the word line are formed with a damascene process.